

system 100, which may include a processor 110, a memory 120, and a network interface 130. The system 100 may also include a display 140 and a user interface 150. The system 100 may be configured to execute a program 160 and store data 170. The system 100 may be connected to a network 180 and a server 190.

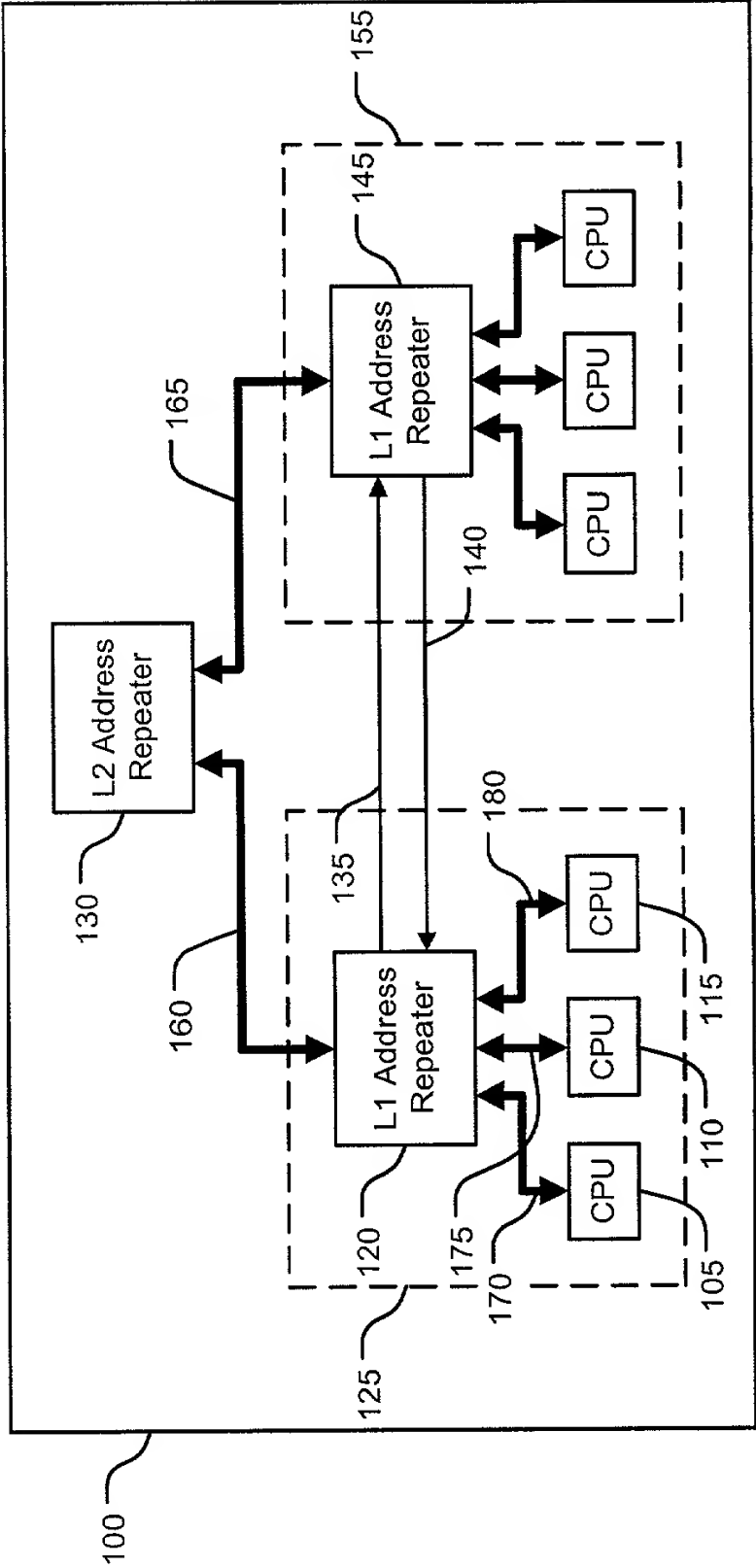


Figure 1

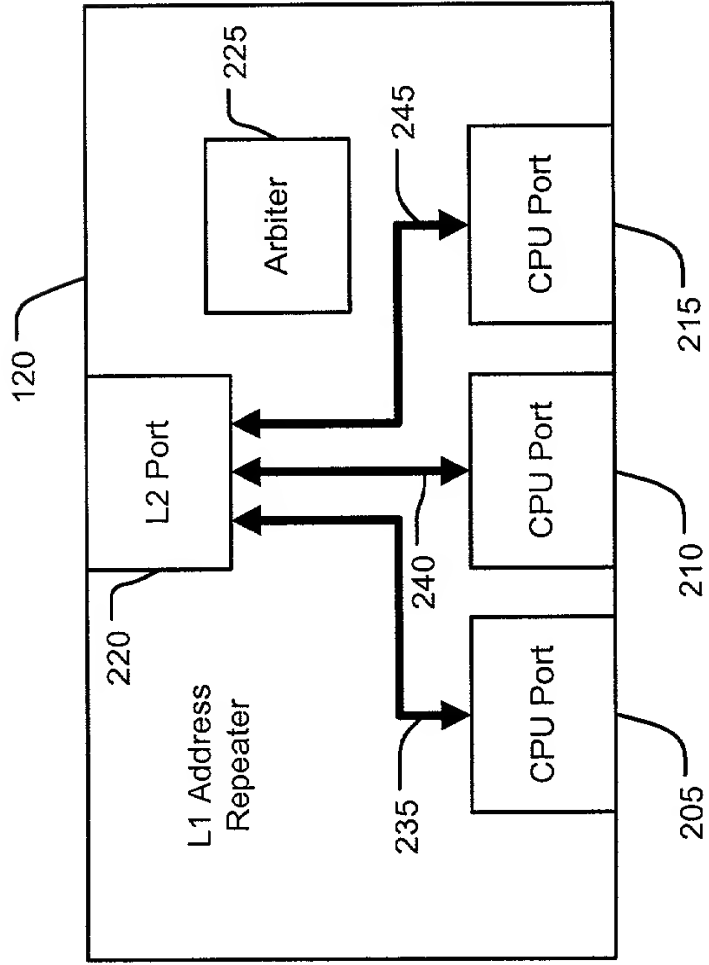


Figure 2

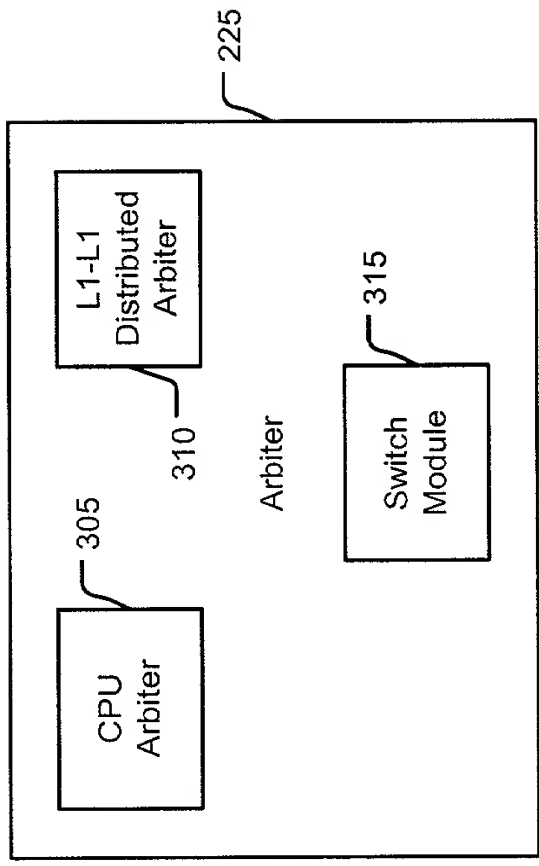


Figure 3

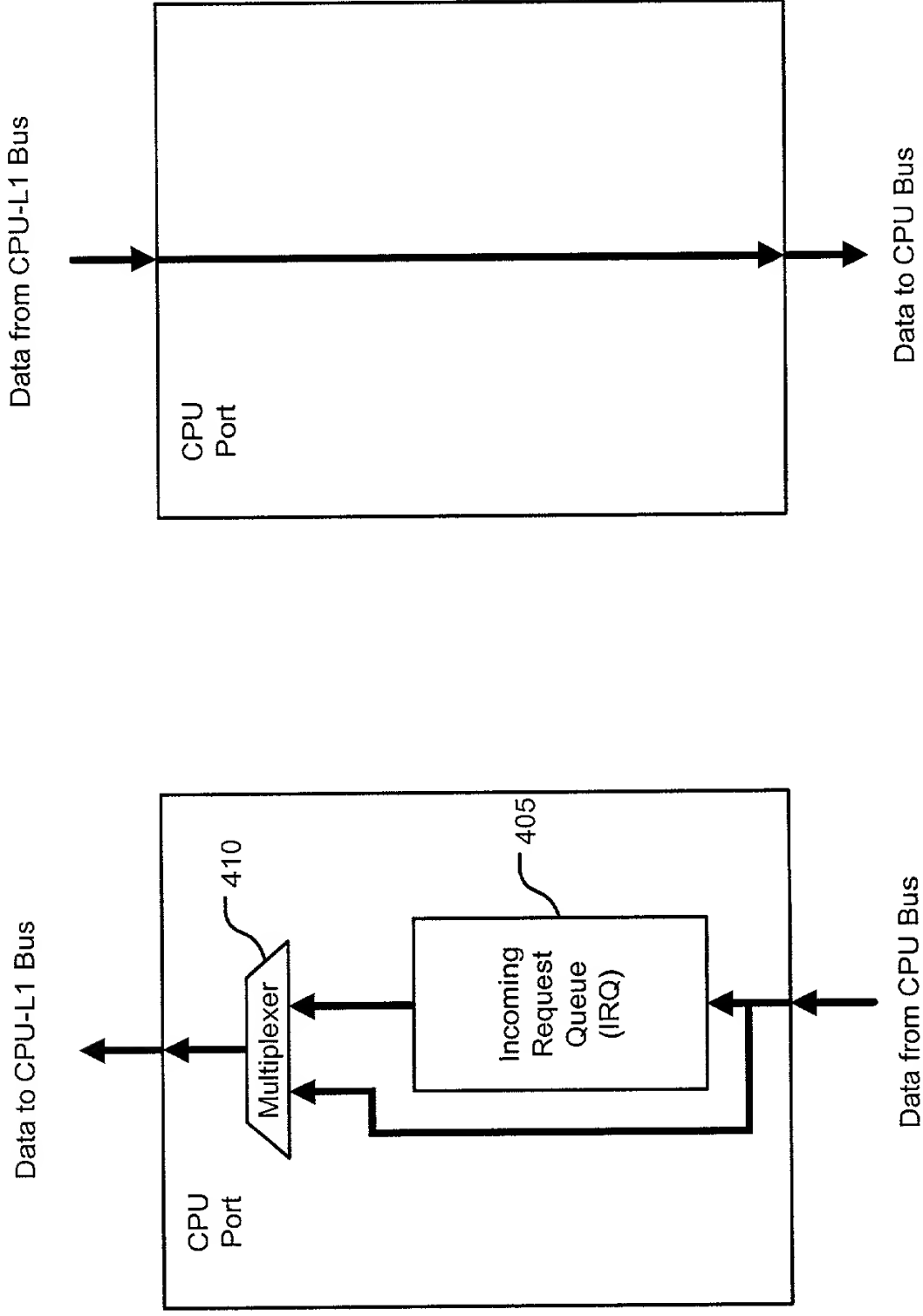


Figure 4(a)

Figure 4(b)

Figure 5 is a block diagram of an L2 Port architecture. The L2 Port is shown as a central block containing an Input Multiplexer (505), an Outgoing Request Queue (ORQ) (510), and an ORQ Multiplexer / Output Demultiplexer (515). Data from L2 Address Repeater enters the L2 Port and is directed to the ORQ Multiplexer / Output Demultiplexer (515). Data from L2 Address Repeater also enters the L2 Port and is directed to the Input Multiplexer (505). The Input Multiplexer (505) receives data from CPU-L1 Bus 235, CPU-L1 Bus 240, and CPU-L1 Bus 245. The ORQ Multiplexer / Output Demultiplexer (515) receives data from the ORQ (510) and outputs data to CPU-L1 Bus 235, CPU-L1 Bus 240, and CPU-L1 Bus 245. The ORQ (510) receives data from the Input Multiplexer (505) and outputs data to the ORQ Multiplexer / Output Demultiplexer (515).

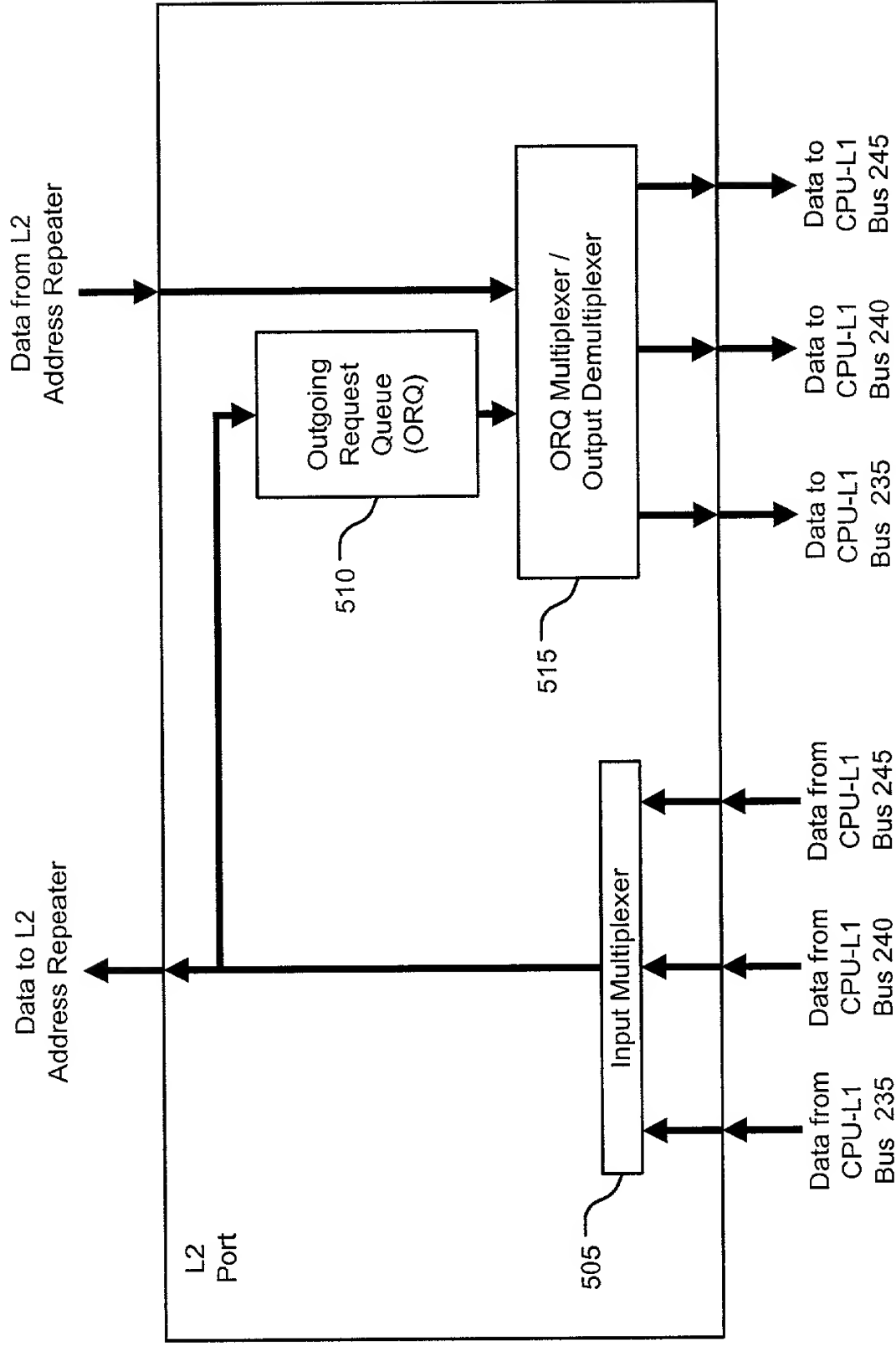


Figure 5

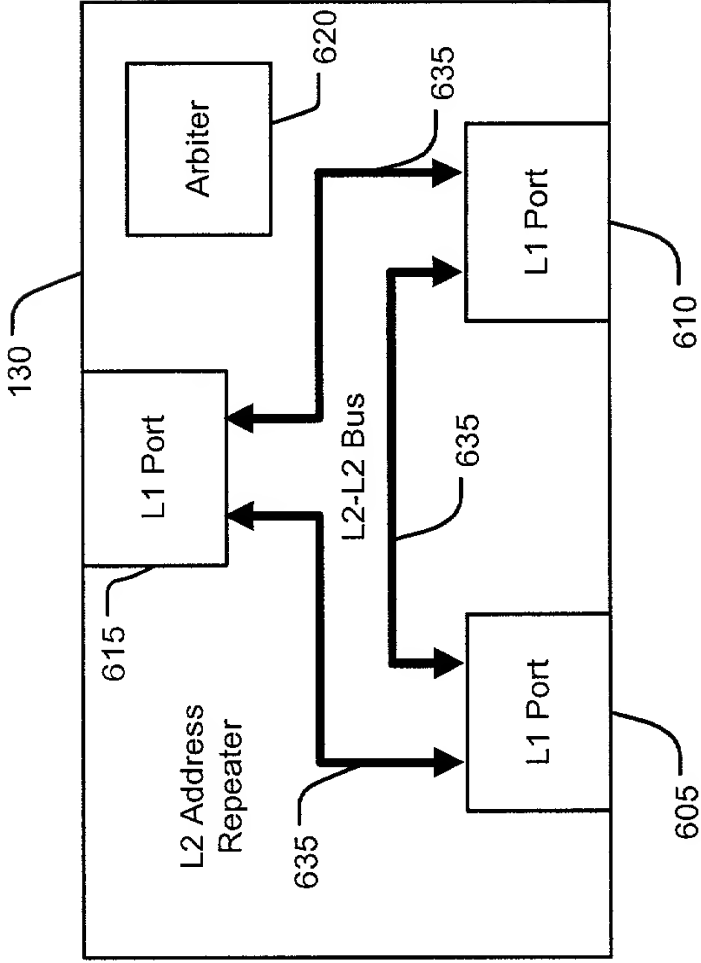
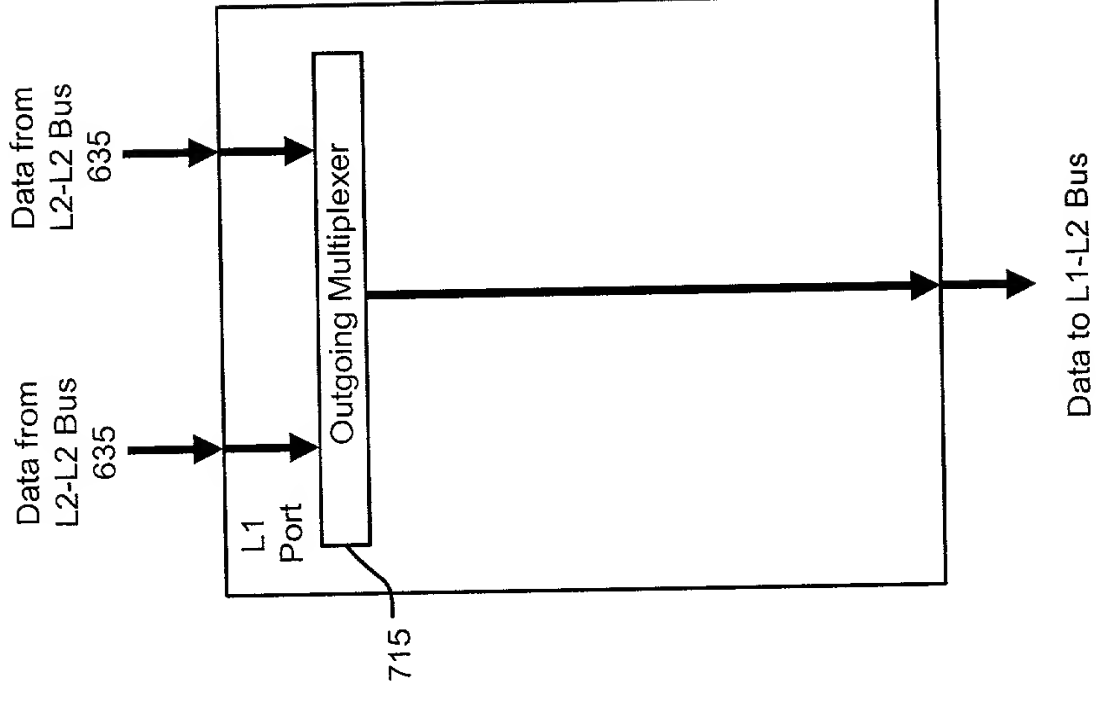
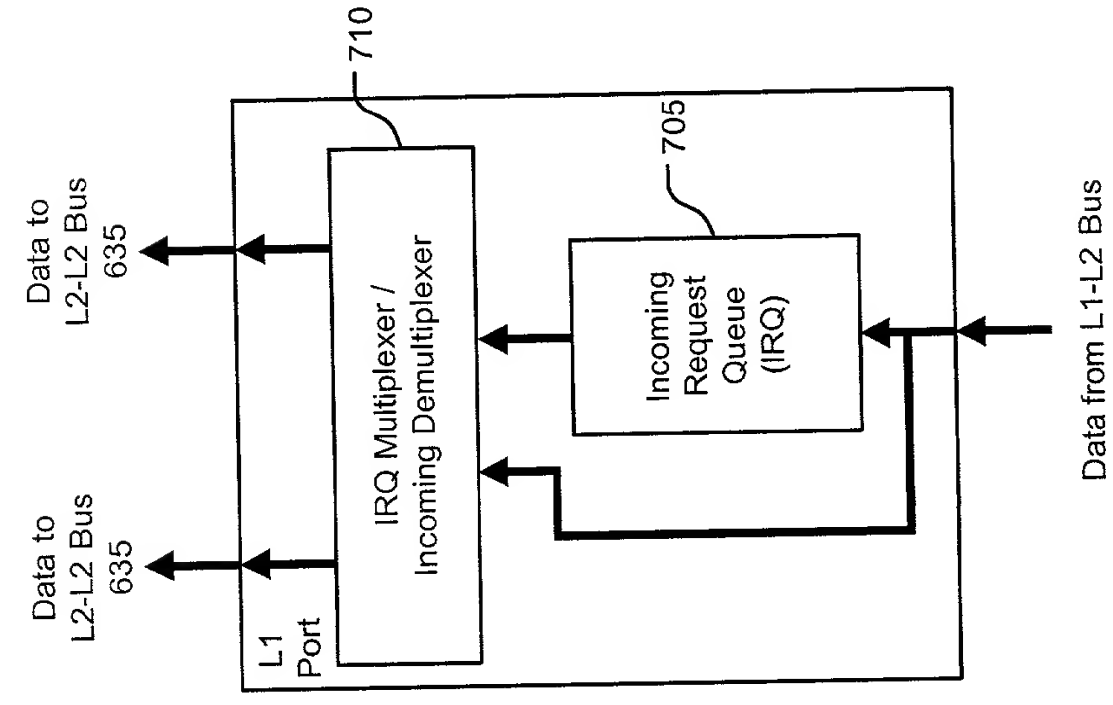


Figure 6



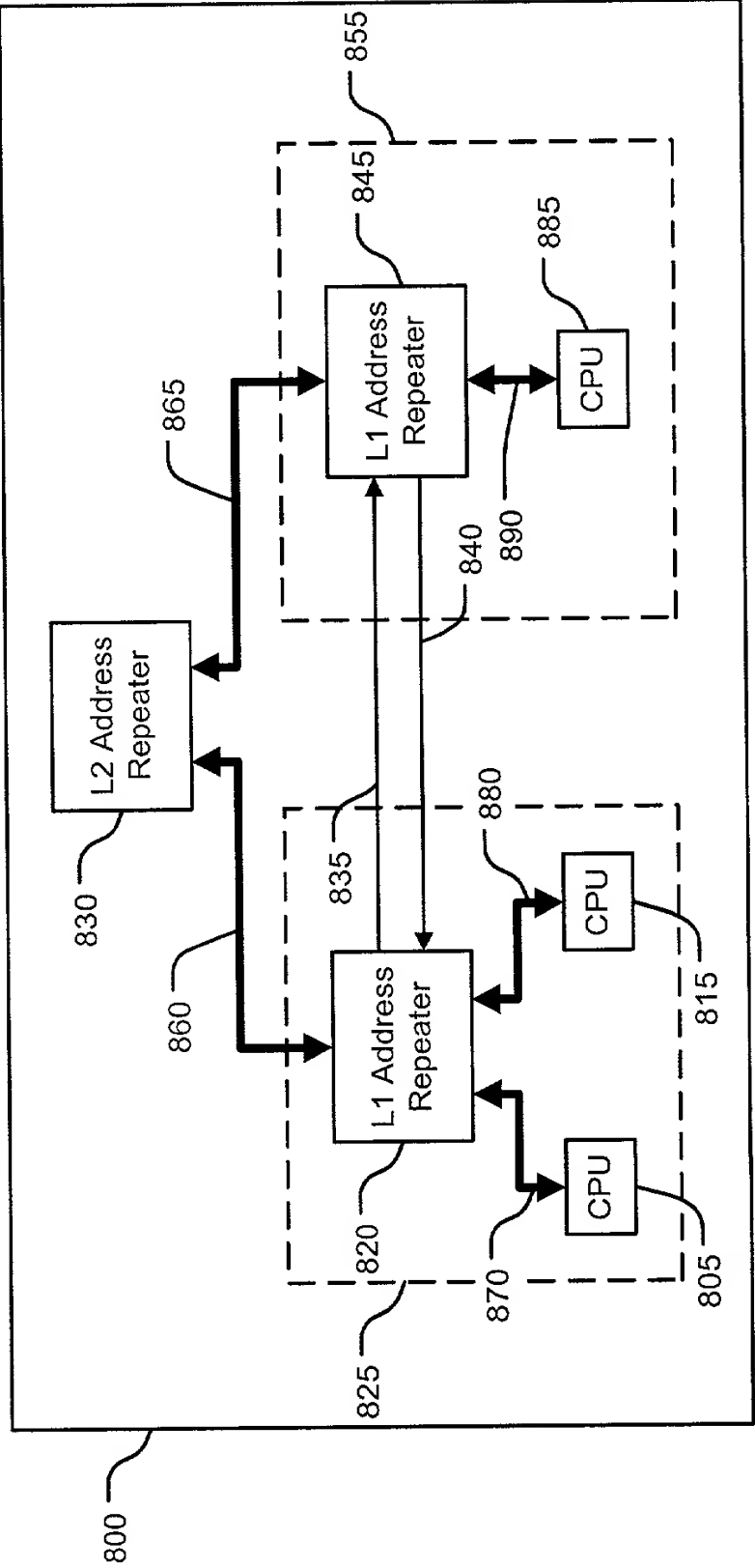


Figure 8

Figure 9 is a timing diagram illustrating the sequence of events for a transaction (Tran A) on a bus system. The diagram shows the interaction between various components over time, with time progressing from left to right.

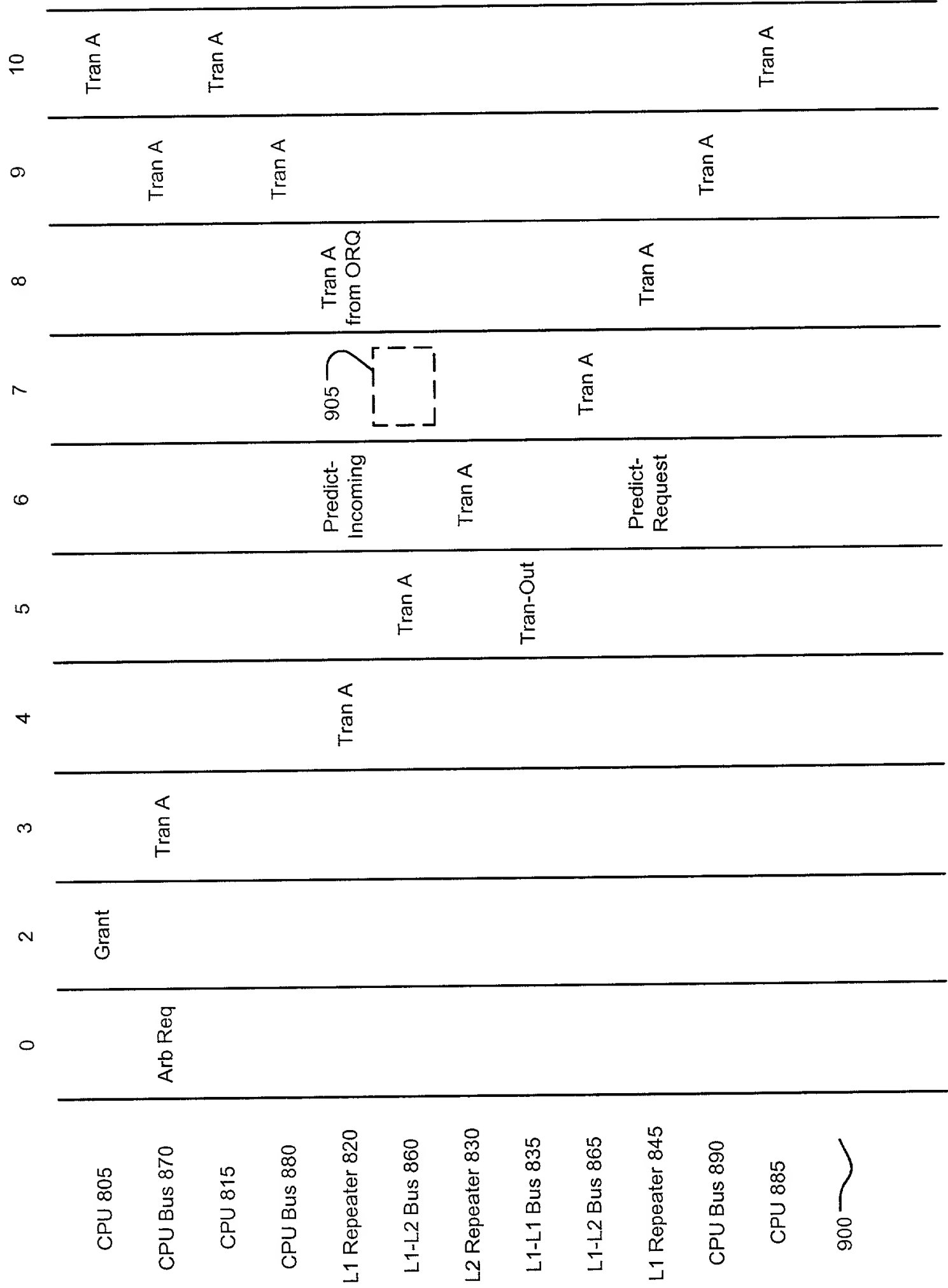


Figure 9